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AMENDMENTS TO THE CLAIMS:

Please cancel claim 27 without prejudice. Please amend the remaining pending claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Currently Amended) An integrated circuit structure, comprising:

a capacitive electrode proximate to a sensing surface on which an object is selectively placed, the capacitive electrode forming a capacitor with the object when the object is placed on the sensing surface;

a dielectric underlying the capacitive electrode; ~~and~~

an a semiconductor device active region underlying the dielectric;

one or more conductive regions extending through the dielectric and between the capacitive electrode and the semiconductor device active region, the one or more conductive regions electrically connecting the capacitive electrode to the semiconductor active region,

wherein the capacitive electrode and ~~all~~ the one or more conductive regions ~~between the capacitive electrode and the active region~~ are formed of a conductive material having a hardness greater than a hardness of aluminum.

2. (Currently Amended) The integrated circuit structure of claim 1, wherein the capacitive electrode and ~~each~~ the one or more conductive regions ~~between the capacitive electrode and the active region~~ are formed of a conductive material having a hardness at least as great as a hardness of the dielectric.

3. (Currently Amended) The integrated circuit structure of claim 1, further comprising:

a passivation layer over the capacitive electrode, the passivation layer forming the sensing surface,

wherein the capacitive electrode and ~~all~~ the one or more conductive regions ~~between the capacitive electrode and the active region~~ are formed of a conductive material having a hardness at least as great as a hardness of the passivation layer.

4. (Currently Amended) The integrated circuit structure of claim 1, wherein the capacitive electrode and ~~all~~ the one or more conductive regions ~~between the capacitive electrode and the active region~~ are formed of tungsten.

5. (Currently Amended) The integrated circuit structure of claim 4, ~~further comprising~~ wherein the one or more conductive regions comprises:

a tungsten via beneath the capacitive electrode.

6. (Currently Amended) The integrated circuit structure of claim 5, ~~further comprising~~ wherein the one or more conductive regions comprises:

a tungsten interconnect beneath the via.

7. (Currently Amended) The integrated circuit structure of claim 6, ~~further comprising~~ wherein the one or more conductive regions comprises:

a tungsten contact between the interconnect and the semiconductor device active region.

8. (Currently Amended) The integrated circuit structure of claim 7, wherein the semiconductor device active region is a gate electrode.

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9. (Withdrawn) An integrated circuit structure, comprising:

~~an~~ a semiconductor device active region;

a dielectric overlying the semiconductor device active region and having a contact opening therethrough;

a tungsten contact within the contact opening and electrically connected to the semiconductor device active region;

a tungsten metal region overlying the tungsten contact and a portion of the dielectric, the tungsten metal region electrically connected to the tungsten contact;

an interlevel dielectric overlying the tungsten metal region and the dielectric and having an opening therethrough;

a tungsten capacitive electrode overlying the tungsten via and a portion of the interlevel dielectric, the tungsten capacitive electrode electrically connected to the tungsten via, wherein the capacitive electrode is proximate to a sensing surface on which an object is selectively placed, the capacitive electrode forming a capacitor with the object when the object is place on the sensing surface ~~and is electrically connected to the active region by the contact, the metal region, and the via.~~

Claims 10–13 (Canceled)

14. (Currently Amended) A method of forming a scratch resistant integrated circuit structure, comprising:

forming ~~an~~ a semiconductor device active region;

forming a dielectric overlying the semiconductor device active region; and

forming a capacitive electrode overlying the dielectric proximate to a sensing surface on which an object is selectively placed, the capacitive electrode forming a capacitor with the object when the object is placed on the sensing surface, wherein the capacitive electrode and ~~each~~ one or more conductive regions ~~between~~ electrically connecting the capacitive electrode ~~and~~ to the semiconductor device active region are formed of a conductive material having a hardness greater than a hardness of aluminum.

15. (Currently Amended) The method of claim 14, wherein the capacitive electrode and ~~each~~ the one or more conductive regions ~~between the capacitive electrode and the active region~~ are formed of a conductive material having a hardness at least as great as a hardness of the dielectric.

16. (Currently Amended) The method of claim 14, further comprising:

forming a passivation layer over the capacitive electrode, the passivation layer forming the sensing surface,

wherein the capacitive electrode and ~~all~~ the one or more conductive regions ~~between the capacitive electrode and the active region~~ are formed of a conductive material having a hardness at least as great as a hardness of the passivation layer.

17. (Currently Amended) The method of claim 14, wherein the capacitive electrode and ~~all~~ the one or more conductive regions ~~between the capacitive electrode and the active region~~ are formed of tungsten.

18. (Currently Amended) The method of claim 17, further comprising:

forming a tungsten via beneath the capacitive electrode and electrically connected to the capacitive electrode.

19. (Currently Amended) The method of claim 18, further comprising:

forming a tungsten interconnect beneath the tungsten via and electrically connected to the tungsten via.

20. (Currently Amended) The method of claim 19, further comprising:

forming a tungsten contact ~~between~~ electrically connecting the tungsten interconnect ~~and~~ to the semiconductor device active region.

21. (Currently Amended) The method of claim 20, wherein the semiconductor device active region is a gate electrode.

22. (Withdrawn) A method of forming an integrated circuit structure, comprising:

forming ~~an~~ a semiconductor device active region;

forming a dielectric overlying the active region and having a contact opening therethrough;

forming a tungsten contact within the contact opening and electrically connected to the semiconductor device active region;

forming a tungsten metal region overlying the tungsten contact and a portion of the dielectric, the tunsten metal region electrically connected to the tungsten contact;

forming an interlevel dielectric overlying the tungsten metal region and the dielectric and having an opening therethrough;

forming a tungsten via within the opening through the interlevel dielectric, the tungsten via electrically connect to the tungsten metal region; and

forming a tungsten capacitive electrode overlying the tungsten via and a portion of the interlevel dielectric, the tungsten capacitive electrode electrically connected to the tungsten via, wherein the capacitive electrode is proximate to a sensing surface on which an object is selectively placed, the capacitive electrode forming a capacitor with the object when the object is placed on the sensing surface ~~and is electrically connected to the active region by the contact, the metal region, and the via~~.

23. (Withdrawn) The method of claim 22, further comprising:

forming an oxide over the capacitive electrode and the interlevel dielectric adjacent the capacitive electrode;

forming a passivation layer including a silicon nitride layer and a silicon carbide layer over the oxide; and

forming tungsten ESD protection within the passivation layer.

24. (Currently Amended) A method of forming a scratch resistant integrated circuit structure, comprising:

forming a plurality of semiconductor device active regions;

forming a dielectric over the plurality of semiconductor device active regions; and

forming an array of capacitive electrodes overlying the dielectric proximate to a sensing surface on which an object is selectively placed, the capacitive electrodes each forming a capacitor with the object when the object is placed on the sensing surface and each electrically connected to a different one of the semiconductor device active regions by one or more conductive conductive regions, wherein the capacitive electrodes and the one or more conductive regions are ~~each~~ formed of a conductive material having a hardness at least as great as a hardness of the dielectric.

25. (Currently Amended) The method of claim 24, ~~wherein the step of forming an array of capacitive electrodes overlying the dielectric of a conductive material having a hardness at least as great as a hardness of the dielectric~~ further ~~comprises~~ comprising:

forming the ~~array of~~ capacitive electrodes and the one or more conductive regions of a conductive material having a hardness at least as great as a hardness of a passivation layer overlying the ~~array of~~ conductive electrodes and forming the sensing surface.

26. (Currently Amended) The method of claim 24, ~~wherein the step of forming an array of capacitive electrodes overlying the dielectric of a conductive material having a hardness at least as great as a hardness of the dielectric~~ further ~~comprises~~ comprising:

forming the ~~array of~~ capacitive electrodes and the one or more conductive regions of tungsten.

Claim 27 (Canceled)